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09/244,270	02/03/1999	LORDSON L. YUE	M-7019-US	3568

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EXAMINER
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CHUNG, DANIEL J

ART UNIT	PAPER NUMBER
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2672

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/244,270

Applicant(s)

YUE ET AL.

Examiner

Daniel J Chung

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 04 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 14-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,14-22 and 24-40 is/are rejected.
- 7) ☒ Claim(s) 23 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

Claims 1-2 and 14-40 are presented for examination. This office action is in response to the RCE filed on 3-4-2005.

#### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3-4-2005 has been entered.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2, 14-22 and 24-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dulia, Jr. et al (6,597,363) in view of Lentz et al (5,446,836).

Regarding claim 1, Dulia, Jr. et al discloses that the claimed feature of a method comprising (See Fig 24, Fig 31, Fig 47-51: receiving vertex data corresponding to the

vertices of a primitive, the vertex data including x-coordinate and y-coordinate position information (See col 44 line 46-49); sorting the vertex data in coordinate dependent fashion [i.e. "VtxYmin, VtxYmax, ...by **sorting the triangle vertices by their y coordinates**", "VtxXmin, VtxXmax...by **sorting the triangle vertices by their x coordinates**", whereas these sorted vertex are used to determine trivially accepted or rejected with respect to tile] (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64); generating region bits [i.e. "outcodes", "numerical numbers (3,1,9,2,8,6,4,12) on divided regions" in Fig 50] representing the location of the sorted vertex data ["sorted vertex"] with respect to a current tile [i.e. 8082 in Fig 50] being rendered [i.e. "outcodes", which generated and used to indicate ***reject primitives that are outside*** ['location of sorted vertex data' in recited claim] ***the view volume*** ['current tile' in recited claim]] (See Fig 50, col 54 line 1-6, col 54 line 14, col 81 line 8-33); generating coordinate data representing an initial rasterization starting point estimate [i.e. "the clipped line start points is generated...a new line start-point ...is generated..."; See col 76 line 30-36, Fig 45] when the region bits indicate that at least one of the sorted vertex data lies within the current tile being rendered [i.e. "trivially accepted primitives", primitives with its edge intersecting a clip plane] and discarding the sorted vertex data of primitives that lie outside the boundary of the current tile being rendered [i.e. "trivially rejected primitives", which are outside the view volume] (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 115 line 53+); and providing the initial rasterization starting point estimate to a rasterizer. (See col 76 line 54-col 77 line15, col 80 line 25-48)

Dulia, Jr. et al does not specifically disclose that “generating coordinate data representing an initial rasterization starting point estimate when one of the sorted vertex data lies within the current tile”. However, such step [‘generating coordinate data for rasterization starting point if the primitive is trivially accepted’] is necessarily required for displaying clipped image in rasterization process. In other word, starting/ending points have to be given or generated, in order to raster any type of polygon/primitives. Therefore, the raster operation of Dulia, Jr. et al inherently meets the limitation in recited claim, as broadly claimed by applicant. **[i.e. the method/function of generating rasterization starting point coordinates are not presented]** Furthermore, as to the teaching of Lentz et al (See “starting points” in Fig 4A and B, where “starting point” in Fig 4B is smarter algorithm of rasterization; See col 3 line 39-45), it would have been obvious to one skilled in the art to incorporate teaching of Lentz (See “starting point” in Fig 4A, Fig 4B, Fig 5, Fig 6, Fig 9, col 3 line 36-col 4 line 46) into the teaching of Dulia, in order to decrease a substantial time of the rasterization efficiently and to minimize computation time for rasterization (by eliminating the image process on invisible side) [i.e. See “In order to reduce the unnecessary processing ...the clipped line start points is generated...a new line start-point ...is generated...” col 76 line 25-36, Fig 45 of Dulia; Also see “smarter algorithm”, “efficient” in col 3 line 39-45 of Lentz], as such improvement [finding starting point for rasterization] is also advantageously desirable in the teaching of Dulia, Jr. et al for rendering the image at faster time by reducing the unnecessary processing of portion of clipped or invisible primitive.

Regarding claim 2, Dulia, Jr. et al disclose that generating an orientation bit representing an orientation of a line connecting the first and second vertices of the sorted primitive with respect to a line connecting the first and third vertices of the sorted primitive before generating the initial rasterization starting point coordinates. (See col 34 line 1-2, col 77 line 26-37) Furthermore, using orientation of triangles to classify or organize the triangle variable or/and calculating an orientation of two side of a triangle is necessarily required for classifying the triangle base on its shape [i.e. right oriented triangle, left oriented triangle], as suggested in the teaching of Lentz (See col 7 line 43-47, col 8 line 24-32), in order to render/raster the triangle/primitives effectively with easy manner.

Regarding claim 14, claim 14 is similar in scope to the claim 1, and thus the rejection to claim 1 hereinabove is also applicable to claim 14.

Regarding claim 15, refer to the discussion for the claim 1 hereinabove, Dulia, Jr. et al discloses that the initial rasterization starting point estimation circuit includes a trivial accept circuit operative to provide the initial rasterization starting point in response to the region bits. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 115 line 53+)

Regarding claim 16, refer to the discussion for the claim 1 hereinabove, Dulia, Jr. et al discloses that the vertex data is sorted in y-coordinate fashion and the trivial accept

circuit provides the x-coordinate and sorted y-coordinate rasterization starting point of a non-discarded primitive. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim 17, refer to the discussion for the claim 1 hereinabove, Dulia, Jr. et al discloses that an interception calculation circuit operative to provide a coordinate dependent initial rasterization starting point in response to the region bits and the vertex data. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 80 line 25-col 82 line 67, col 115 line 53+)

Regarding claim 18, refer to the discussion for the claim 1 hereinabove, Dulia, Jr. et al discloses that the boundary interception point generated by the intercept calculation circuit represents the initial rasterization point starting point coordinate. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 80 line 25-col 82 line 67, col 115 line 53+)

Regarding claim 19, refer to the discussion for the claim 1 hereinabove, Dulia, Jr. et al discloses that an interception calculation circuit operative to provide a coordinate dependent initial rasterization starting point in response to the region bits and the sorted vertex data. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 80 line 25-col 82 line 67, col 115 line 53+)

Regarding claim 20, refer to the discussion for the claim 1 hereinabove, Dulia, Jr. et al discloses that the trivial accept circuit comprises a logic gate coupled to a corresponding subset of the region bits. (See col 125 line 16-col 126 line 33)

Regarding claim 21, refer to the discussion for the claim 1 hereinabove, Dulia, Jr. et al discloses that the logic gate is an AND gate. (See col 125 line 16-col 126 line 33)

Regarding claim 22, Dulia, Jr. et al discloses that the region bits define the top edge, bottom edge, right edge and left edge of a current tile being rendered. (See Fig 50)

Regarding claim 24, refer to the discussion for the claim 1 hereinabove, Dulia, Jr. et al discloses that the x-coordinate and y-coordinate of the initial rasterization starting point to the boundary intercept points. (See col 34 line 11-56, col 77 line 44-col 78 line 20, col 80 line 25-col 82 line 67, col 115 line 53+)

Regarding claim 25, claim 25 is similar in scope to the claim 2, and thus the rejection to claim 2 hereinabove is also applicable to claim 25.

Regarding claim 26, refer to the discussion for the claim 1 hereinabove, Dulia, Jr. et al discloses that determining the relative positioning between the vertices of the primitive. (See col 34 line 11-13, col 34 line 34-36, col 44 line 46-64)



Regarding claims 27-28, claims 27-28 are similar in scope to the claim 1, and thus the rejection to claim 1 hereinabove is also applicable to claims 27-28.

Regarding claim 29, Dulia, Jr. et al discloses that the position data includes x coordinate and y coordinate position data, and the sorting step comprises arranging the position data in y coordinate order. [i.e. "VtxYmin, VtxYmax, ...by sorting the triangle vertices by their y coordinates"] (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim 30, Dulia, Jr. et al discloses that the primitive are arranged in descending y coordinate order. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim 31, Dulia, Jr. et al discloses that the primitives are arrange in ascending y-coordinate order. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim 32, Dulia, Jr. et al discloses that the position data includes x coordinate and y coordinate position data, and the sorting step comprises arranging the position data in x coordinate order. [i.e. "VtxXmin, VtxXmax...by sorting the triangle

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vertices by their x coordinates] (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim 33, Dulia, Jr. et al discloses that the primitive are arranged in descending x coordinate order. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim 34, Dulia, Jr. et al discloses that the primitives are arrange in ascending x-coordinate order. (See col 34 line 11-13, col 34 line 34-36, col 44 line 50-64)

Regarding claim 35, Dulia, Jr. et al discloses that comparing the x coordinate position data with the corresponding coordinate position data of the current tile; and discarding the primitive when the x coordinate position is greater than the largest corresponding coordinate position of the current tile. (See col 3 line 44-col 4 line 1, "clipping test" in claims 1,4-5, 18-19)

Regarding claim 36, Dulia, Jr. et al discloses that comparing the x coordinate position data with the corresponding coordinate position data of the current tile; and discarding the primitive when the x coordinate position is less than the smallest corresponding coordinate position of the current tile. (See col 3 line 44-col 4 line 1, "clipping test" in claims 1,4-5, 18-19)

Regarding claim 37, Dulia, Jr. et al discloses that comparing the y coordinate position data with the corresponding coordinate position data of the current tile; and discarding the primitive when the y coordinate position is greater than the largest corresponding coordinate position of the current tile. (See col 3 line 44-col 4 line 1, "clipping test" in claims 1,4-5, 18-19)

Regarding claim 38, Dulia, Jr. et al discloses that comparing the y coordinate position data with the corresponding coordinate position data of the current tile; and discarding the primitive when the y coordinate position is less than the smallest corresponding coordinate position of the current tile. (See col 3 line 44-col 4 line 1, "clipping test" in claims 1,4-5, 18-19)

Regarding claim 39, Dulia, Jr. et al discloses that generating an initial x coordinate and an initial y coordinate based on the corresponding x coordinate and sorted y coordinate of the primitive within the current tile. (See col 76 line 25-36, Fig 45, Also See "starting points" in Fig 4A and B, where "starting point" in Fig 4B is smarter algorithm of rasterization; col 3 line 39-45 in Lentz et al)

Regarding claim 40, Dulia, Jr. et al discloses that generating the initial x coordinate and y coordinate based on the boundary region of the current tile. (See col 76 line 25-36, Fig 45, Also See col 3 line 39-45 in Lentz et al)

***Allowable Subject Matter***

Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Amendment/Argument***

In Recent Applicant's Remarks, Applicant argued that the cited reference do not disclose "generating an initial rasterization starting point estimate when the sorted vertex data lies within the tile boundary and discarding the sorted vertex data that lie outside of the tile boundary" of recited claims, (See Remarks p.9 line 12-15, p.11 line 4-6) because the cited references (Dulia and Lentz) describe starting the rasterization of a triangle at a point outside of the triangle rather than an initial rasterization starting point estimate within the current tile. However, it is noted that the features upon which applicant relies (i.e. 'an initial rasterizaztion starting point within the current tile') are not recited in the rejected claim(s). The presented claims only describe that 'generating an initial rasterization starting point if at least one of primitive's vertex data lies within the current tile ' [i.e. 'trivially accepted primitives' or 'primitives with its edge intersecting current tile's boundary'] and 'discarding vertex data of primitive lie outside current tile' [i.e. "trivially rejected primitives"] Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Chung whose telephone number is (703) 306-3419. He can normally be reached Monday-Thursday and alternate Fridays from 7:30am- 5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael, Razavi, can be reached at (703) 305-4713.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks  
Washington, D.C. 20231


**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

djc  
April 14, 2005



MICHAEL J. FORD  
SUPERVISOR PATENT EXAMINER